REMARKS

In the non-final 25 January 2006 *Office Action*, the Examiner rejects Claims 1-20. Applicant thanks the Examiner with appreciation for the careful consideration and examination given to the Application.

After entry of this Response, Claims 1-20 are pending in the Application. Applicant respectfully asserts that Claims 1-20 are in condition for allowance and respectfully request reconsideration of the claims in light of the following remarks.

The undersigned respectfully requests a telephonic conference with the Examiner regarding the following remarks and the cited references.

I. Pending Claims & Present Invention

As the Examiner will recall, embodiments of Applicant's invention can provide an apparatus that causes invalid data to be read again from a memory device before being read by a device. The apparatus can include a transaction queue to store pending and dispatched device transactions. The apparatus can also include a controller to respond to an invalid data signal by preventing the transaction queue from dispatching pending transactions to the memory device by causing the transaction queue to dispatch again the device read transaction which resulted in the invalid data and, subsequently, by causing the data which was read again from the memory device to be accepted by the destination device, by setting the dispatched transaction pointer to the pending transactions pointer, and by enabling the transaction queue to dispatch pending transactions to the memory device.

Applicant's currently pending claims recite various features directed to retrying a read transaction. Advantageously, Applicant's claimed invention enables a device read transaction to be performed a second time if a previous device read transaction results in invalid data. (*Specification*, Paragraphs 6-10). In addition, Applicant's claimed invention enables a memory system to flag a memory location as providing invalid data so that future write operations to a erroneous memory location is disabled until valid data is read from the erroneous memory location. (*Specification*, Paragraphs 39-40). As discussed in detail below, Applicant respectfully submits that the references of record do not render Applicant's claims unpatentable.

Importantly, the cited references do not mention, discuss, disclose, or fairly suggest each and every element and limitation of Applicant's currently pending claims. For example, the

references do not disclose an apparatus adapted to: dispatch a pending transaction to a device, dispatch a device read transaction resulting in an invalid data signal and, subsequently, to that sending to a desired destination a data available signal for data resulting from a device read transaction which was dispatched again, and dispatch a pending transaction to the device.

In addition, the references do no teach or fairly suggest receiving an indication that data read from a device location is not valid, inhibiting write operations to the device, reading the data from that device location again; and enabling write operations to the device, and sending to a desired destination a valid data signal for the data which resulted from reading that device location again as currently claimed by Applicant.

For at least these reasons and the below-discussed reasons, Applicant respectfully asserts that Claims 1-20 are patentable over the cited references.

II. 35 U.S.C. § 102 Rejection

The Examiner rejects Claims 1-14, 16-18 and 20 under 35 U.S.C. § 102(b) as allegedly being anticipated by *Hagerston* (USPN 5,829,033). The Examiner asserts that *Hagerston* discloses the subject matter contained in Claims 1-14, 16-18 and 20. Applicant respectfully traverses the § 102 rejection because *Hagerston* does not disclose each and every claimed element and limitation as required by § 102(b).

Hagerston discloses a system for optimizing responses in a coherent distributed electronic system including a computer system. A main objective of *Hagerston's* system is to provide a system for updating cache memory systems to include the same data so that multiple caches are coherent. (Column 3, Lines 1-45). *Hagerston's* objective is quite different from those of Applicant's currently claimed invention, which includes retrying a device read transaction to correct a previous invalid data error.

Hagerston's system provides a ReadToShareFork ("RTSF") transaction that ***simultaneously*** causes a write-type operation that updates invalid data from a requested memory address, and provides the updated data to the requesting device. (Column 5, Lines 34-45). More specifically, when writing valid data to memory, the RTSF transaction simultaneously causes reissuance of the originally requested transaction using the same memory address and ID information. (*Id.*). The requesting device upon recognizing its transaction ID on the bus system will pull the now valid data from the desired memory location. (*Id.*). Indeed, when valid data is

written to a requested memory location to update memory, an outstanding read-type transaction is caused to reissue, using the same memory address and transaction information. (Column 4, Line 65 – Column 5, Line 8). By sending the valid data to two destinations simultaneously, both "transactions" occur simultaneously. (*Id.*).

Importantly, however, *Hagerston* does not teach or fairly suggest several advantageous features and limitations appearing in Applicant's claims. Notably, *Hagerston* lacks any discussion of an apparatus having the features claimed by Applicant in Claims 1 and 7. For example, *Hagerston* does not teach or fairly suggest an apparatus having a transaction queue adapted to: being prevented from dispatching a pending transaction to a device, dispatching again a device read transaction to a memory location which resulted in an invalid data signal and, subsequently, dispatching a pending transaction to the device.

Further, *Hagerston* is not even remotely closely related to solving the problems solved by Applicant's claimed invention, which include reading a memory device location multiple times in an attempt to correctly read data which may have become unstable or corrupt due to a transient such that a second or successive data read may result in correct data being read.

The Examiner asserts that Column 19, Lines 4-24 of *Hagerston* anticipate certain features claimed by Applicant in Claims 1, 7, 13, and 17. Applicant respectfully disagrees. As discussed above, this portion of *Hagerston* discloses a RTSF transaction. But the RTSF transaction does not teach what Claims 1, 7, 13, and 17 recite. For example, the RTSF transaction can write and read at the same time. Applicant claims no such feature.

Rather Applicant claims holding any pending transactions upon discovering invalid data to retry a read transaction. Further, Applicant claims rereading a memory location providing invalid data, and then subsequently, sending to a desired destination a data available signal for the data which resulted from data reread, and dispatch pending transaction. The RTSF transaction does not disclose such features, and therefore fails to anticipate Applicant's claimed invention. Indeed, the RTSF transaction does not teach to retry a read transaction while holding pending data transactions, and then, subsequently, dispatching the held data transactions after retrying a read transaction.

Applicant also respectfully asserts that Claims 13 and 17 are allowable for additional reasons. Both Claims 13 and 17 recite "inhibiting write operations to the device." The Examiner asserts that Column 24, Lines 65-67 teach such claimed feature. This disclosure, however, does

not disclose inhibition of write operations; rather it discloses a coding scheme permitting devices to distinguish between error types. (Column 25, Lines 1-2).

Applicant also respectfully asserts that certain dependent claims are allowable. For example, Claims 6 and 16 are not anticipated by *Hagerston*. The Examiner asserts that a portion of Hagerston that reads: "The Mapped signal preferably allows sufficiently lengthy timeouts to be treated as fatal hardware errors rather than as nonfatal errors" anticipates Claims 6 and 16. Such is not the case. Claims 6 and 16 recite that the invalid data has an uncorrectable error. This portion of *Hagerston* fails to even mention data, much less data having an uncorrectable error. Accordingly Claims 6 and 16 are patentable over *Hagerston*.

For at least the above reasons, Applicant respectfully asserts that Applicant's currently claimed invention (Claims 1-22) is allowable over *Hagerston*. Withdrawal of the § 102 rejection is respectfully requested.

III. 35 U.S.C. § 103 Rejection

The Examiner asserts that Claims 15 and 19 are unpatentable under 35 U.S.C. § 103. Specifically, the Examiner asserts that a combination of *Hagerston* and *Brzezinski* (USPN 5,570,297) renders Claims 15 and 19 unpatentable.

Applicant respectfully traverses the § 103 rejections in light of the above-presented remarks regarding *Hagerston*. Because *Hagerston* fails to teach each and every claimed limitation of the independent claims and *Brzezinski* does not overcome the deficiencies of *Hagerston*, the asserted § 103 rejection also fails to teach the subject matter as a whole as claimed in dependent Claims 15 and 19. Accordingly, Applicant respectfully asserts that Claims 15 and 19 are allowable over the cited combination for at least this reason.

Applicant also respectfully asserts that Claim 15 and 19 are allowable for additional reasons. Applicant respectfully submits that the Examiner has not set forth a *prima facie* case of obviousness. As MPEP § 2143 provides, a *prima facie* of obviousness requires three findings. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art must teach or suggest all the claim limitations.

Applicants respectfully submit that the cited combination does not provide the requisite

motivation/suggestion as required by MPEP § 2143. Indeed, one of ordinary skill in the art would not find any motivation in the cited references to combine them as does the Examiner. Not only are the cited references non-analogous art, they are directed to solving very different technical problems from each other and Applicant's claimed invention. For example, *Hagerston* discloses a system for optimizing responses in a coherent distributed electronic system including a computer system, and *Brzezinski* discloses a system to synchronize wireless data transfer between a wrist watch and a video screen. Those skilled in the art to which the Applicant's currently claimed invention is directed (memory controllers and memory systems) would not turn to *Hagerson* or *Brzezinski* for guidance since both references are directed at solving problems not pertinent to the problems solved by Applicant's currently claimed invention. Thus, the cited references can not be properly combined to sustain a § 103 rejection.

In addition to not providing the requisite motivation, the § 103 rejection lacks other requirements necessary for a proper § 103 rejection. Indeed, the Examiner provides no reasonable expectation of success that Applicant's claimed invention as recited in Claims 15 and 19 would result from the cited combination. Moreover, the cited combination does not teach or suggest all the claim limitations. The portions of *Brzezinski* of cited by the Examiner fail to teach the subject matter appearing in Claims 15 and 19. More specifically, *Brzezinski* discloses to test for a stop bit. If a stop bit is not received then an error flag is set, and if a stop bit is received no flag is set or an error flag is cleared.

This *Brzezinski* disclosure does not anticipate Claims 15 and 19. Claims 15 and 19 recite "if invalid data read from that device location has not occurred previously then setting a previous error flag to indicate that invalid data from that device location has occurred previously" and "if invalid data read from that device location has occurred previously then clearing the previous error flag to indicate that invalid data from that device location has not occurred previously." This claimed subject matter is not taught in *Brzezinski* because *Brzezinski* discloses the opposite of what Applicant claims. Applicant claims to set a previous error flag if an invalid data read has not occurred previously and to clear the previous error flag if an invalid data read has occurred. Further, *Brzezinski*'s flag does not indicate whether or not invalid data from a device location has or has not occurred as claimed by Applicant.

Accordingly, the Examiner has not set forth a *prima facie* case of obviousness. Applicant, therefore, respectfully submits that Claims 15 and 19 are allowable over the cited

combination. Withdrawal of the § 103 rejection is respectfully requested.

V. Fees

Applicant files this Response within three months of the 25 January 2006 Office Action and with no additional claims. Accordingly, Applicant believes that no extension or claims fees are due. The Commissioner is authorized, however, to charge any fees that may be required, or credit any overpayment, to Deposit Account No. 20-1507.

VI. Conclusion

The foregoing is believed to be a complete response to the non-final *Office Action* mailed 25 January 2006. Applicant respectfully asserts that Claims 1-20 are in condition for allowance and respectfully requests passing of this case in due course of patent office business. If the Examiner believes there are other issues that can be resolved by a telephone interview, or there are any informalities remaining in the application which may be corrected by an Examiner's amendment, a telephone call to Hunter Yancey at (404) 885-3696 is respectfully requested.

Respectfully submitted,

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